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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DUONG, KHANH B	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,867	KONG ET AL.	
	Examiner	Art Unit	
	Khanh B. Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7,13,16-22,24-33 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,13,16-22,24,25 and 42* is/are rejected.

7)☒ Claim(s) *26-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 21, 2005 has been entered.

Response to Amendment

Accordingly, claims 1, 6, 13, 16, 18-21, 24, 26, 29, 32, 33 and 42 were amended, and new claim 42 was added

Currently, claims 1, 4-7, 13, 16-22, 24-33 and 42 are pending in the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 19-22 and 24-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 19 recites the limitation "the data wire" in lines 15 to 16. There is insufficient antecedent basis for this limitation in the claim.

*** Other claims are rejected as depending on the rejected base claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 4-7 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (US 6,433,842) in view of Fogarty et al. (US 4,181,564).

Kaneko et al. ("Kaneko") discloses in FIG. 1 a method for manufacturing a wire contact structure, comprising steps of: forming a first conductive layer (8 and 9) formed of an aluminum-based material (8); depositing a silicon nitride layer 10 on the wire (8 and 9) at a temperature of 230°C; forming a contact hole 19 extending through the silicon nitride layer 10 and exposing the first conductive layer (8 and 9); and forming a second conductive layer 11 formed of indium zinc oxide (IZO) and directly contacting the first conductive layer (8 and 9) through the contact hole 19.

Re claims 1, 4 and 5, Kaneko discloses depositing the silicon nitride insulating layer 10 at a temperature of 230°C instead of between about 280°C and about 400°C for about 5 minutes to

about 40 minutes. Kaneko also fails to disclose the contact hole having a size between about 0.5 mm x 15 μm and 2 mm x 60 μm.

Fogarty et al. ("Fogarty") suggests forming a silicon nitride layer at a temperature between 270°C and 375°C and for a period of about 45 minutes [see col. 2, line 65 to col. 3, line 3 and col. 4, lines 35-55].

Since Kaneko and Fogarty are both from the same field of endeavor, the purpose disclosed by Fogarty would have been recognized in the pertinent prior art of Kaneko.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Kaneko as suggested by Fogarty, since Fogarty states at column 4, lines 26-29 such modification would provide a silicon nitride layer having an essentially constant Si/N ratio throughout the thickness of the layer.

Furthermore, with respect to process parameters such as temperature, time and size, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the process parameters within the ranges as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Re claims 6 and 7, since the contact structure of the first conductive layer (8 and 9) of Kaneko are formed of the same materials (aluminum) as the claimed invention, it should be inherent that a contact resistance between the first conductive layer (8, 9) and the second conductive layer 11 is less than 10% of a resistance of the first conductive layer or less than 0.15 $\mu\Omega cm^2$.

Re claim 42, see discussions above regarding claims 1, 4 and 5. Kaneko further discloses in FIG. 1 the following steps: depositing a first conductive layer (8 and 9) formed of aluminum (portion 8) on a substrate 1; inherently patterning the first conductive layer (8 and 9) to form a "signal line"; depositing a silicon nitride layer 10 on the "signal line" at a fixed temperature of 230°C; forming a contact hole 19 extending through the silicon nitride layer 19 and exposing the "signal line"; forming a second conductive layer 11 formed of indium zinc oxide (IZO) and directly contacting the "signal line" through the contact hole 19.

Claims 13 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. (US 6,163,356) in view of Kaneko and Fogarty.

Song et al. ("Song") discloses in FIG. 4a to 4f a method for manufacturing a thin film transistor array panel, comprising steps of: depositing a first conductive layer formed of an aluminum-based material on a substrate 1; patterning the first conductive layer to form a gate line 13a and a gate pad 15a connected to the gate line 13a; depositing a silicon nitride layer 17 on the gate line 13a and a gate pad 15a; forming a semiconductor layer (33, 35) on the silicon nitride layer 17; depositing a second conductive layer (21 and 31) on the semiconductor layer (33, 35); patterning the second conductive layer (21 and 31) to form a "data line"; forming a contact hole 59 extending through the silicon nitride 17 and exposing the gate pad 15; depositing a third conductive layer formed of an ITO layer; and patterning the third conductive layer to form a conductive pattern 57 directly contacting the gate pad 15 in the contact hole 59 [see col. 4, line 30 to col. 5, line 67].

Re claim 13, Song fails to disclose the following: depositing the silicon nitride gate insulating layer at a temperature between about 280°C and about 400°C, and depositing an indium zinc oxide (IZO) layer to form the third conductive layer.

Fogarty suggests forming a silicon nitride layer at a temperature in the range of 270-375°C for a period in the range of about 45 minutes [see col. 2, line 65 to col. 3, line 3 and col. 4, line 35-55]. However, Forgarty does not mention the use of IZO as a conductive layer. Kaneko suggests in FIG. 1 depositing either an indium tin oxide (ITO) layer or an indium zinc oxide (IZO) layer over the passivation layer 10 so as to form a pixel electrode 11.

Since Song, Fogarty and Kaneko are from the same field of endeavor, the purpose disclosed by Fogarty and Kaneko would have been recognized in the pertinent prior art of Song.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Song as suggested by Fogarty, since Fogarty states at column 4, lines 26-29 such modification would provide a silicon nitride layer having an essentially constant Si/N ratio throughout the thickness of the layer. In addition, because ITO and IZO were art-recognized equivalent materials as demonstrated by Kaneko at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute one material for the other.

Furthermore, with respect to process parameters such as temperature, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the process parameters within the ranges as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Re claim 18, Song expressly discloses in Fig. 4f the step of patterning the third conductive layer comprises a step of forming a pixel electrode 41 connected to the "data line" 31.

Re claim 19, see discussions above regarding claim 13. Song further discloses in FIG. 4a to 4f a method for manufacturing a thin film transistor array panel, comprising steps of: depositing a first conductive layer formed of an aluminum-based material on a substrate 1; patterning the first conductive layer to form a gate line 13, a gate electrode 11 and a gate pad 15; depositing a silicon nitride layer 17; forming a semiconductor layer (33, 35) on the silicon nitride layer 17; depositing a second conductive layer over the silicon nitride layer 17 and the semiconductor layer (33, 35); patterning the second conductive layer to form a data line 23, a source electrode 21, a drain electrode 31; forming a passivation layer 37 over the silicon nitride layer 17; forming a contact hole 59 extending through the passivation layer 37 and the silicon nitride layer 17 and exposing the gate pad 15; depositing a third conductive layer formed of an ITO layer over the passivation layer 37; and patterning the third conductive layer to form a redundant gate pad 57 directly contacting the gate pad 15 through the contact hole 59 [see col. 4, line 30 to col. 5, line 67].

Re claim 20, Song expressly discloses in Fig. 4f patterning the third conductive layer to form a pixel electrode 41.

Re claim 21, Song expressly discloses in Fig. 4d patterning the second conductive layer to form a data pad 25, and patterning the third conductive layer to form a redundant data pad 67 connected to the data pad 25.

Re claim 22, Song discloses the passivation layer 37 comprises silicon nitride [see col. 5, lines 12-15] but does not mention any specific temperature range for forming the silicon nitride. See discussion above for claim 13 regarding the formation of silicon nitride within a specific temperature range.

Claims 16, 17, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song, Fogarty and Kaneko as applied to claims 13 and 18-22 above, and further in view of Arai et al. (US 6,399,222).

Re claims 16, 17, 24 and 25, the combined disclosure of Song, Fogarty and Kaneko does not specifically mention the third conductive layer (IZO) is formed by sputtering target including In_2O_3 and ZnO, wherein the content of Zn in a compound of In_2O_3 and ZnO is in the range of 15-20%.

Arai et al. ("Arai") suggests the indium zinc oxide is preferably formed by sputtering target including In_2O_3 and ZnO, wherein the content of Zn in a compound of In_2O_3 and ZnO is in the range of 1-20% [see col. 4, line 22-32].

Since Song, Fogarty, Kaneko and Arai are from the same field of endeavor, the purpose disclosed by Arai would have been recognized in the pertinent prior art of Song, Fogarty and Kaneko.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined process of Song, Fogarty and Kaneko as suggested by Arai, since Arai states at column 4, lines 47-49 that such modification would provide an electrode layer having a sufficient thickness.

Furthermore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select an appropriate content of Zn in a compound of In_2O_3 and ZnO within the range as taught by Arai. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Allowable Subject Matter

Claims 26-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed October 21, 2005, with respect to the amended claims, have been fully considered but they are not persuasive.

Applicant argues that Kaneko fails to disclose or suggest "forming a contact hole ... exposing the first conductive layer" and "forming a second conductive layer ... directly

contacting the first conductive layer through the contact hole". In response, the Examiner respectfully disagrees since Kaneko clearly discloses in FIG. 1 forming a contact hole 19 exposing the first conductive layer (combination of layers 8 and 9) and forming a second conductive layer 11 directly contacting the first conductive layer through the contact hole 19.

Applicant further argues that, in Kaneko, "the contact hole formed in the passivation layer 10 ... does not expose the aluminum alloy layer 8" and "the ITO pixel electrode 11 ... does not directly contact the aluminum alloy layer 8". In response, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It appears that Applicant had equated the limitation "a first conductive layer formed of an aluminum-based material" to that of a single layer comprising 100% of an aluminum-based material. Such limitation can be interpreted as single layer comprising multiple sublayers, wherein the sublayers comprise an aluminum-based material and other materials.

In regard to Song, Applicant argues "the contact hole 59 does not expose the aluminum gate pad 15a". In response, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Again, it appears that Applicant had equated the limitation "a first conductive layer formed of an aluminum-based material" to that of a single layer comprising 100% of an aluminum-based material. Such limitation can be interpreted as single layer comprising multiple

sublayers, wherein the sublayers comprise an aluminum-based material and other materials. In this case, Song can be interpreted to disclose a first conductive layer (combination of 15 and 15a) comprising of an aluminum-based material 15a. Thus, it can be understood that the contact hole 59 exposes the gate pad (combination of 15 and 15a).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following U.S. Patents teach relevant information regarding forming a redundant gate pad on and in direct contact with a gate pad: Park '883 [see at least FIG. 7E] and Jang '666 [see Fig. 16].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KBD

Zandra V. Smith
Supervisory Patent Examiner
6 March 2006